UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,676	07/02/2003	Thomas C. Anthony	10014296-1	3426

7590 09/08/2005

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400

EXAMINER	
TRAN, LONG K	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 09/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/612,676	ANTHONY ET AL.	
	Examiner	Art Unit	
	Long K. Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 18-32* is/are pending in the application.

4a) Of the above claim(s) *18 - 28* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 – 12 and 29 – 32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on June 07, 2005 has been entered.

Response to Amendment

2. This office action is in response to Amendment filed on June 07, 2005;

3. Claims **13 – 17** and **33** have been cancelled.

4. Claims **1, 29** and **30** have been amended.

5. Claims **18 – 28** have been withdrawn.

6. Claims **1 – 12** and **29 – 32** are presented for examination.

7. This is a new ground of rejection.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims **1 – 12** and **29 – 32** are rejected under 35 U.S.C. 103(a) as being unpatentable over Rizzo et al. (US Patent Application Publication No. 2004/0000415) in view of Rostoker et al. (US Patent No. 5,389,556).

10. Regarding claim **1**, Rizzo discloses a semiconductor device 5 (fig. 1, [0030]) comprising:

a first surface 17 (figs. 1 – 5 and 7 – 9) having memory chips 15 (figs. 2 – 4; only one shown; [0025], [0039] and [0003]) disposed thereon, the memory chips defining an exterior face 18 (figs. 1 – 5 and 7 – 9; [0026]) of the semiconductor device;

a second surface 21 (figs. 5 and 7 – 9; [0028]) opposite the exterior face 18; and

A magnetically permeable shield layer 26 (figs. 7 – 9; [0032], [0033] and [0043]) extending over the entirety of the second surface 21.

However, as noted, Rizzo fails to disclose that the semiconductor device 5 including memory chips/dies 15 as a wafer having unseparated memory chips as claimed in the instant claim.

Nevertheless, at the time the invention was made, in order to form a plurality of identical chips/dies, one would form the identical chips/dies from a semiconductor wafer having unseparated chips before being cut into individual chip/die. One would do that because that was how one of the ordinary skills in the art would do also shown by Rostoker (column 1, lines 10 – 15).

Regarding claim **2**, Rizzo and Rostoker disclose the memory chips are separable from the memory wafer (Rizzo: [0039] and Rostoker, column 1, lines 15 – 17).

Regarding claim **3**, Rizzo discloses memory chips 15 (figs. 1 – 2; [0025]) are MRAM.

Regarding claim **4**, Rizzo discloses the memory chips 15 include multiple memory arrays having multiple memory cells 14 (figs. 1 – 5 and 7 – 9; [0025]).

Regarding claim **5**, Rizzo discloses memory cells 14 are MRAM cells ([0025]).

Regarding claims **6** and **7**, Rizzo discloses the memory chips 15 include contact/bond pads (at the edges of the chips not shown; [0025], [0030] and [0049]) electrically accessible via the exterior face of the memory wafer.

Regarding claims **8** and **9**, Rizzo discloses the magnetically permeable shield layer 26 comprises a soft material selected from the group consisting of alloys of iron, alloys of nickel and alloys of cobalt ([0033]).

Regarding claim **10**, Rizzo et al. disclose the magnetically permeable shield layer 26 has a permeability of greater than 100 ([0042] and [0053]).

Regarding claim **11**, Rizzo et al. disclose the magnetically permeable shield layer has a coercivity of less than 10 Oersteds ([0043] and [0047]).

Regarding claim **12**, Rizzo et al. disclose the magnetically permeable shield layer is isotropic ([0053]).

11. Regarding claims **29** and **30**, Rizzo discloses a semiconductor device 5 (fig. 1, [0030]) comprising:

a first surface 17 (figs. 1 – 5 and 7 – 9) having memory chips 15 (figs. 2 – 4; only one shown; [0025], [0039] and [0003]) disposed thereon, the memory chips defining an exterior face 18 (figs. 1 – 5 and 7 – 9; [0026]) of the semiconductor device;

a second surface 21 (figs. 5 and 7 – 9; [0028]) opposite the exterior face 18; and

A magnetically permeable shield layer 26 comprises a soft material selected from the group consisting of alloys of iron, alloys of nickel and alloys of cobalt (figs. 7 – 9; [0032], [0033] and [0043]) extending over the entirety of the second surface 21. *Note that the magnetically permeable shield layer 26 is considered means for protecting the memory chips from external or stray magnetic filed ([0003], [0006] and [0010]).*

Rizzo fails to disclose that the semiconductor device 5 including memory chips/dies 15 as a wafer having unseparated memory chips as claimed in the instant claim.

However, at the time the invention was made, in order to form a plurality of identical chips/dies, one would form the identical chips/dies from a semiconductor wafer having unseparated chips before being cut into individual chip/die. One would do that because that was how one of the ordinary skills in the art would do also shown by Rostoker (column 1, lines 10 – 15).

Regarding claim **31**, Rizzo et al. disclose the magnetically permeable shield layer 26 has a permeability of greater than 100 ([0042] and [0053]).

Regarding claim **32**, Rizzo et al. disclose the magnetically permeable shield layer has a coercivity of less than 10 Oersteds ([0043]).

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ray et al. (US Patent No. 6,921,965) discloses a memory device having a layer with high magnetic permeability for shielding the semiconductor device from stray or external magnetic fields similar to that of Rizzo et al. (US Patent

Application Publication No. 2004/0000415) and Rostoker et al. (US Patent No. 5,389,556).

13. A shortened statutory period for response to this action is set to expire e (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02 (b)).

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long K. Tran whose telephone number is 571-272-1797. The examiner can normally be reached on Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LKT

August 22, 2005